REMARKS

This Amendment addresses the issues outstanding from the final Office Action of November 30, 2007. Applicants respectfully request favorable reconsideration of this application, as amended.

As a preliminary matter, Applicants wish to thank Examiner Karimi for confirming (in a voice message on April 10, 2008) receipt of priority Japanese Patent Application No. 2003-160538. Formal acknowledgement in the next official communication is respectfully requested.

By this Amendment, independent Claims 22, 27, and 34 have been amended to recite certain distinctive features of Applicants' invention with greater particularity, as will be discussed below; Claim 30 has been amended to change its dependency to Claim 28; and Claims 24, 29, and 36 have been cancelled without prejudice or disclaimer. Claims 1-21 were previously cancelled without prejudice or disclaimer. Accordingly, Claims 22, 23, 25-28, and 30-35 are pending, with Claims 22, 27, and 34 being independent.

In the final Office Action, Claims 22-36 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Kanatani in view of Sakaguchi.

Without acceding to the rejection, Applicants have amended the independent claims to recite certain distinctive

features of Applicants' invention with greater particularity. Claim 22, for example, has been amended additionally to recite that converting the display data includes: (1) setting one specified bit of the display data to logic "0" by a first exclusive logic circuit when the switching signal and the one specified bit match each other, (2) setting the one specified bit to logic "1" by the first exclusive logic circuit when the switching signal and the one specified bit do not match each other, (3) setting each of other bits of the display data to logic "1" by an associated second exclusive logic circuit of a plurality of second exclusive logic circuits when the one specified bit matches the other bit, and (4) setting each of other bits of the display data to logic "0" by the associated second exclusive logic circuit when the one specified bit does not match the other bit, whereby the first display data and the second display data are in the same bit pattern except for the one specified bit when converting the display data.

The Kanatani and Sakaguchi references cited in the outstanding rejection are not seen to teach or suggest the foregoing features of Applicants' invention, as now set forth in Claim 22.

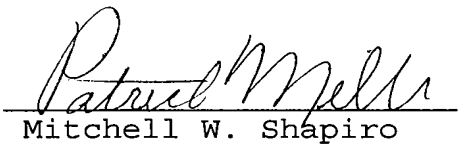
Independent apparatus Claims 27 and 34 have been amended in an analogous manner to Claim 22 and thus

similarly distinguish from the collective disclosures of Kanatani and Sakaguchi.

In view of the foregoing, favorable action is respectfully requested.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 (XA-10079) any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account. If any extension of time is required in connection with the filing of this paper and has not been separately requested, such extension is hereby requested.

Respectfully submitted,

By: 

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